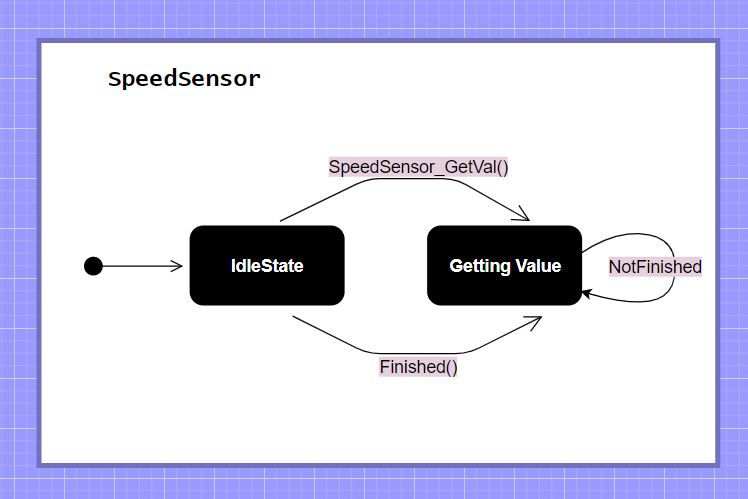
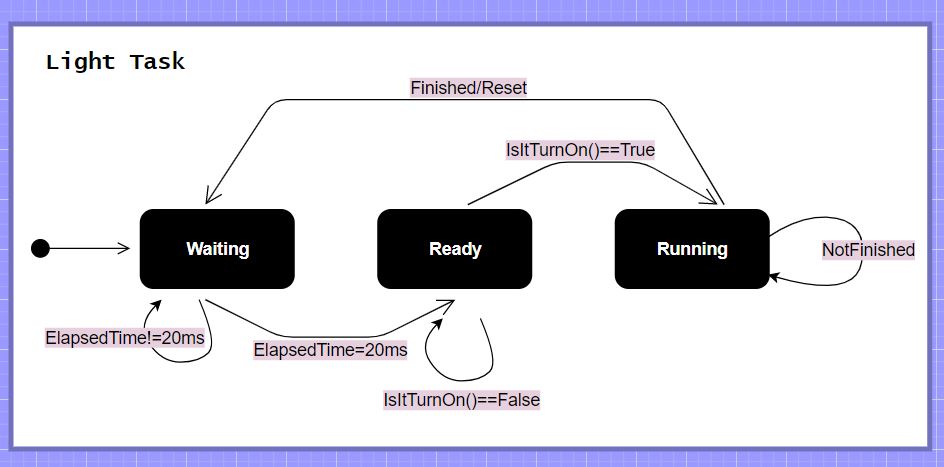
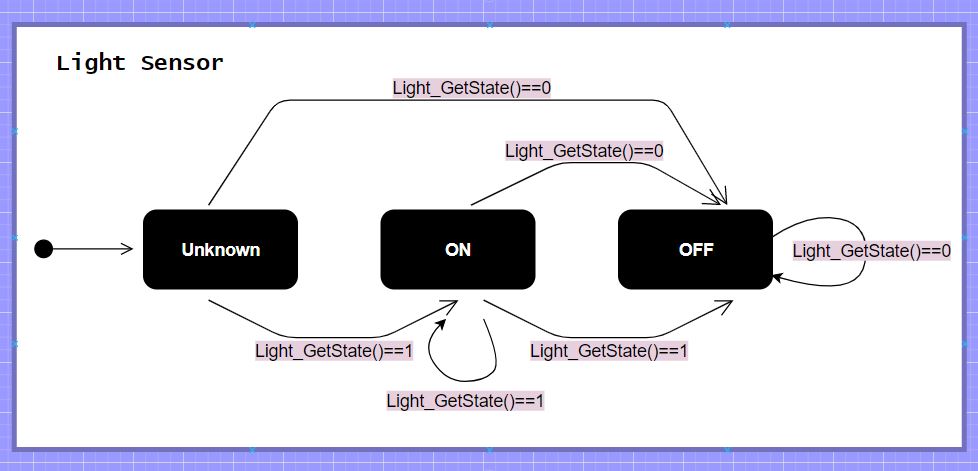
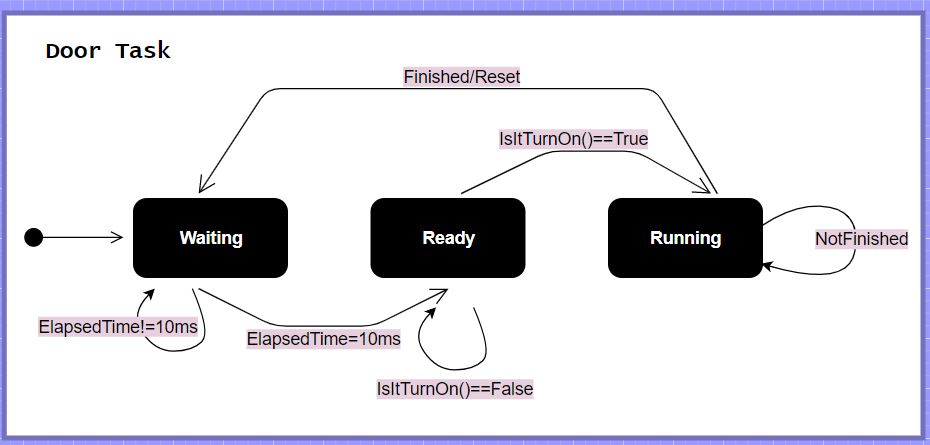
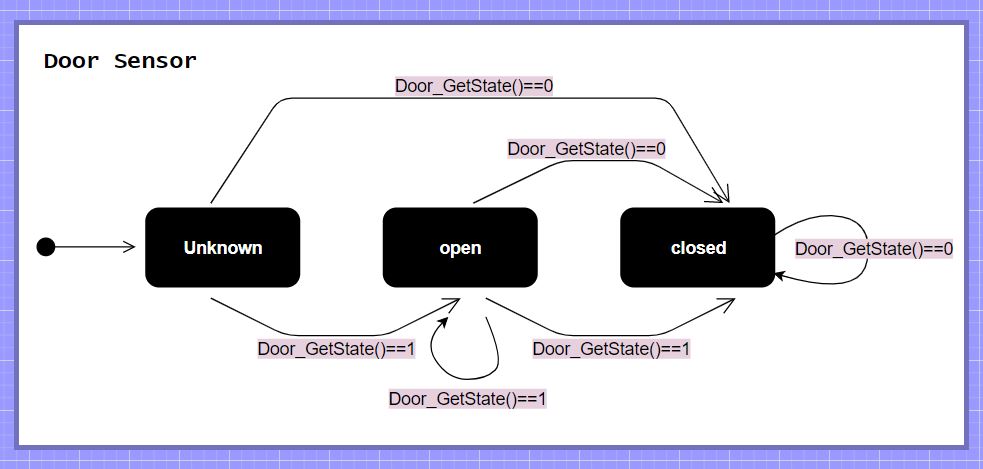
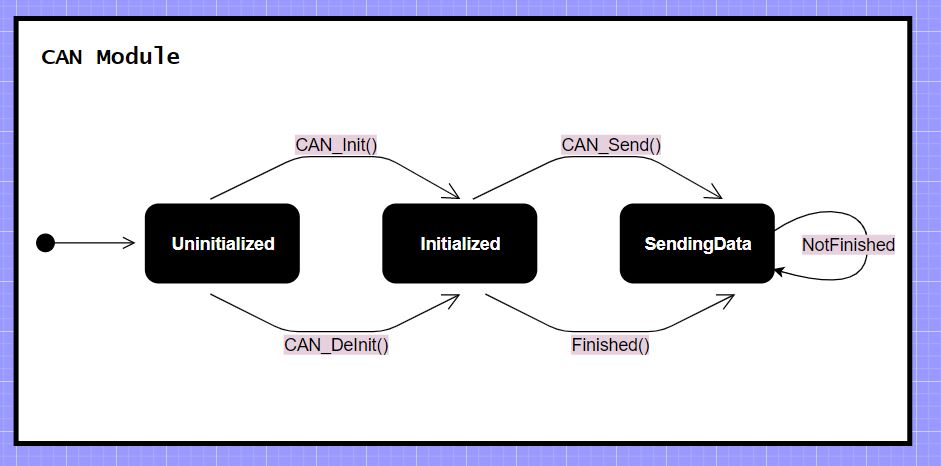
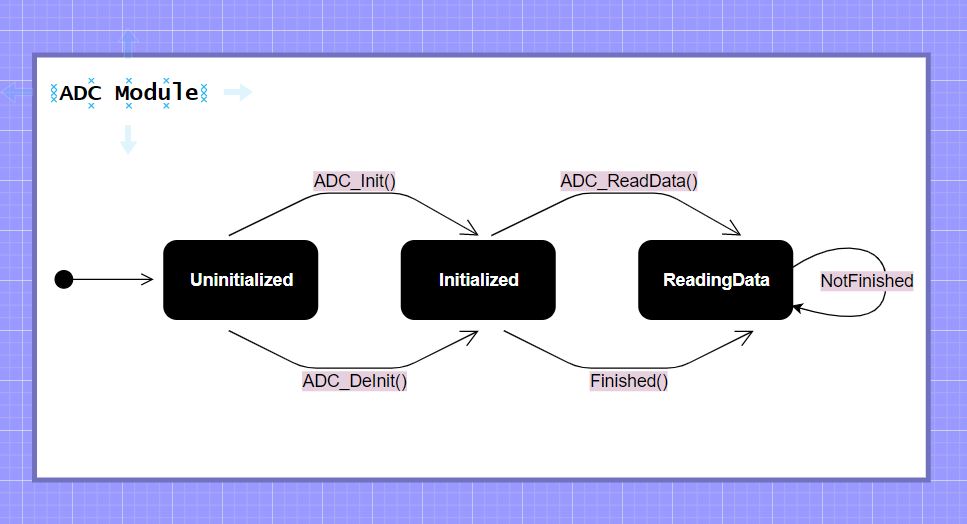
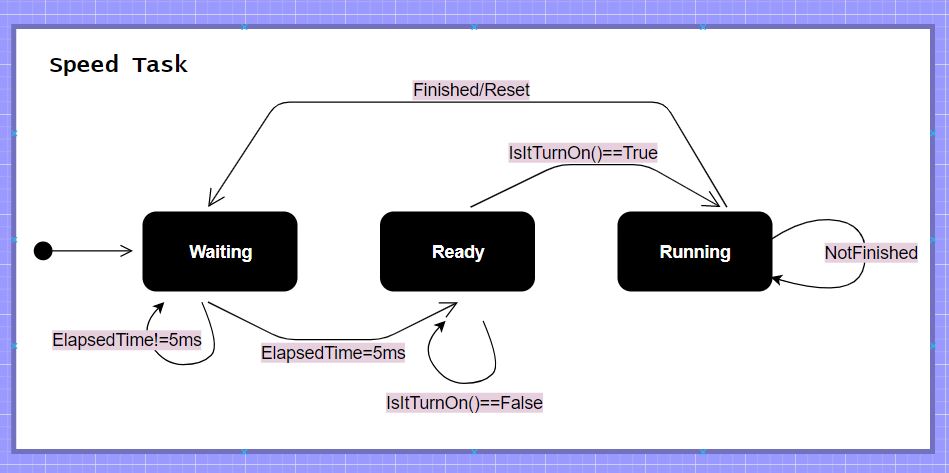
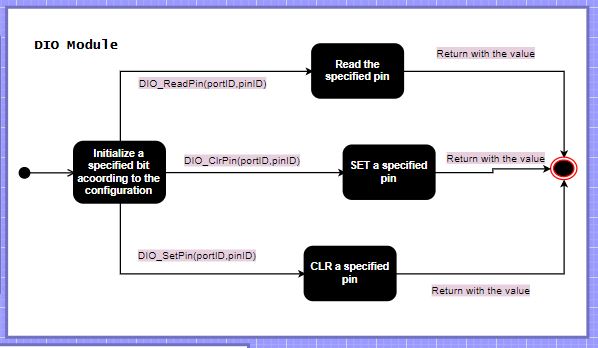
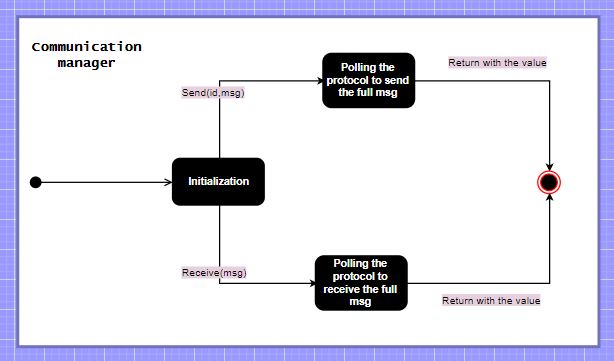
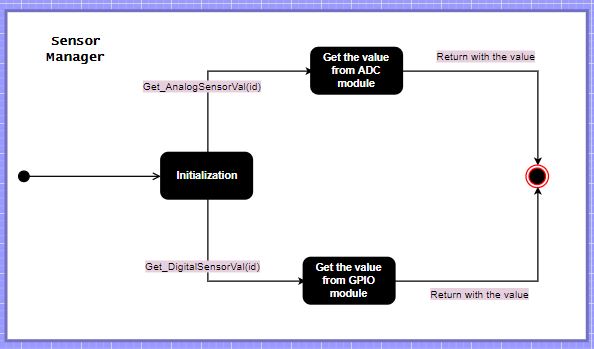
Dynamic Design

# ECU1:

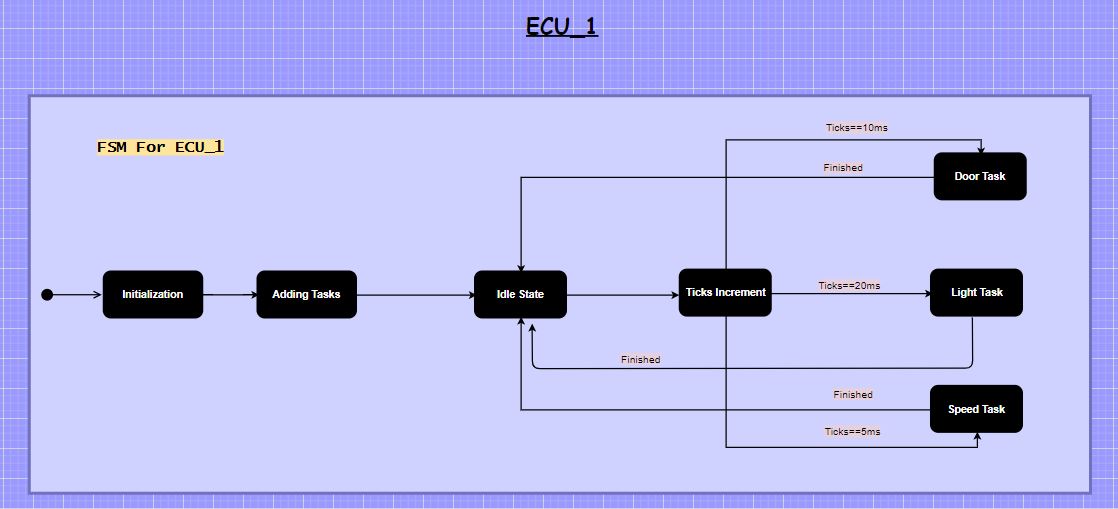
## FSM for each component of ECU1:



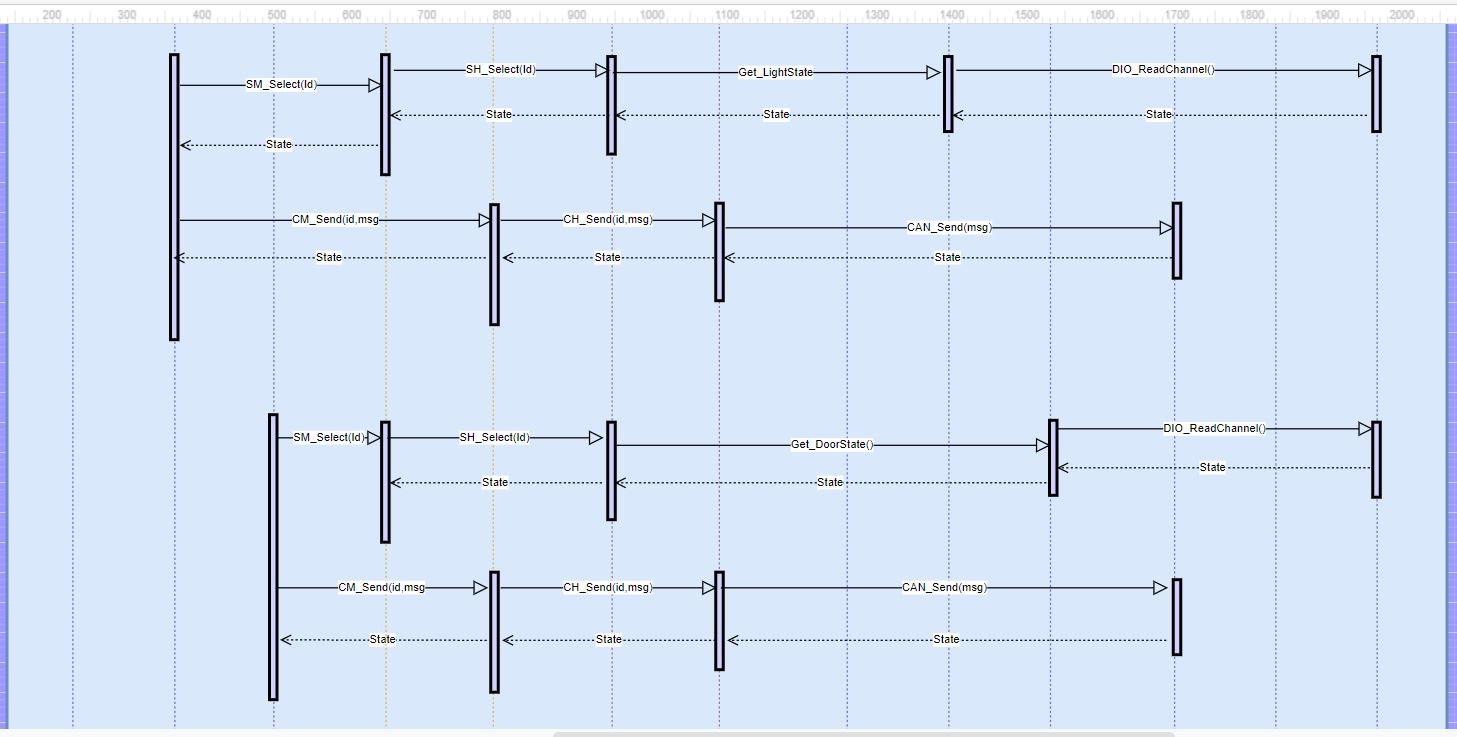
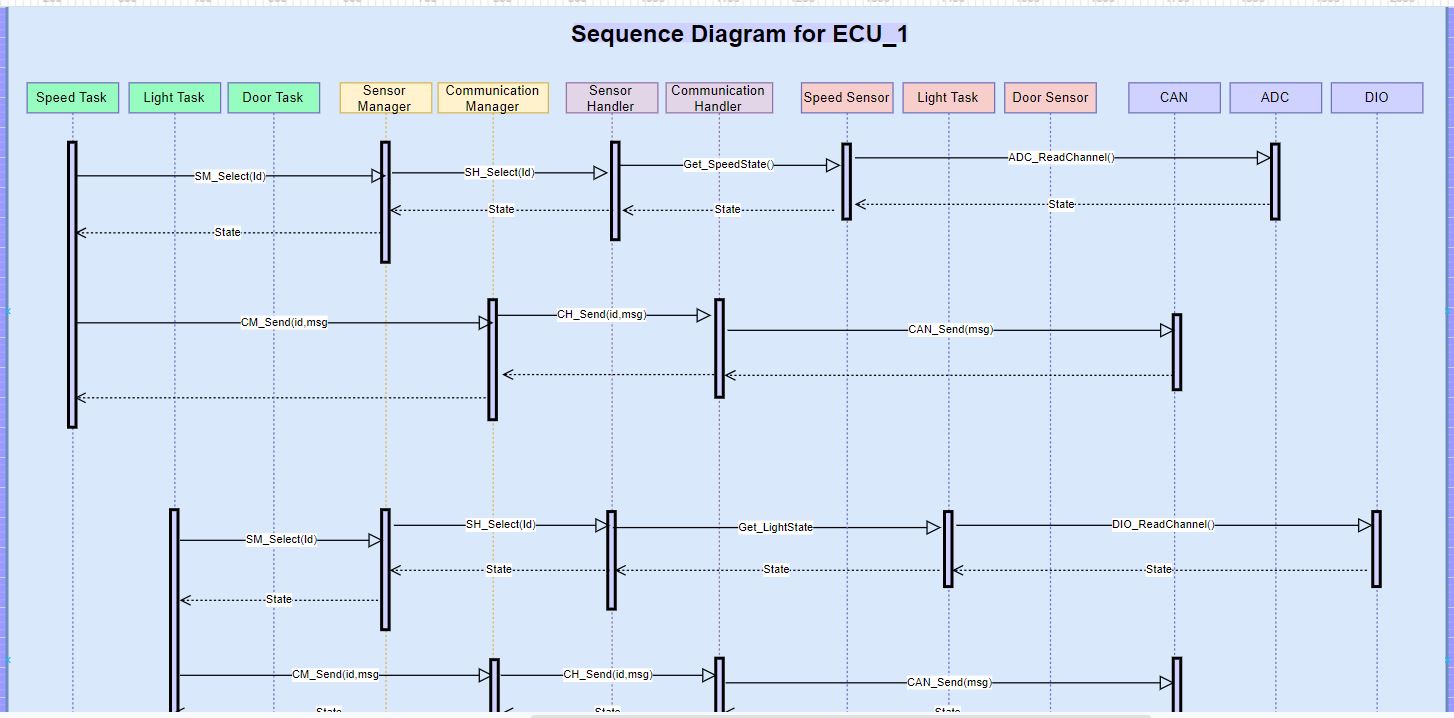




## FSM for ECU1:



## Sequence Diagram:



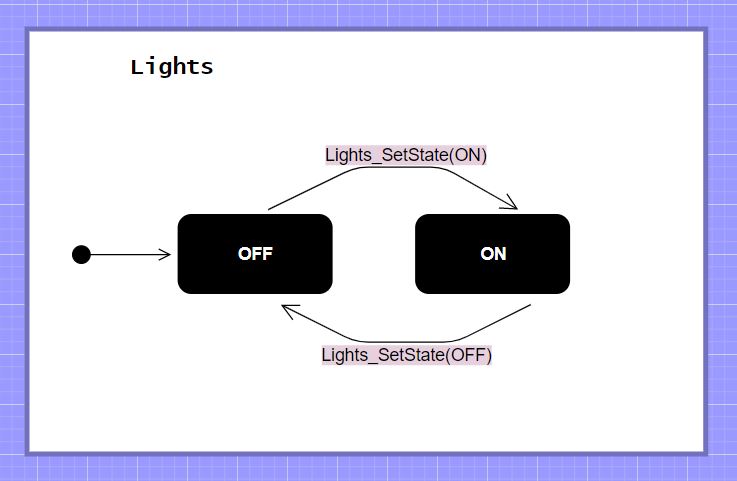
## CPU Load:

Assuming all tasks execution time = 1ms:

U = (E1 + E2 + E3)/H = (1 ∗ 1 + 1 ∗ 2 + 1 ∗ 4)/20) ∗ 100 = 35%

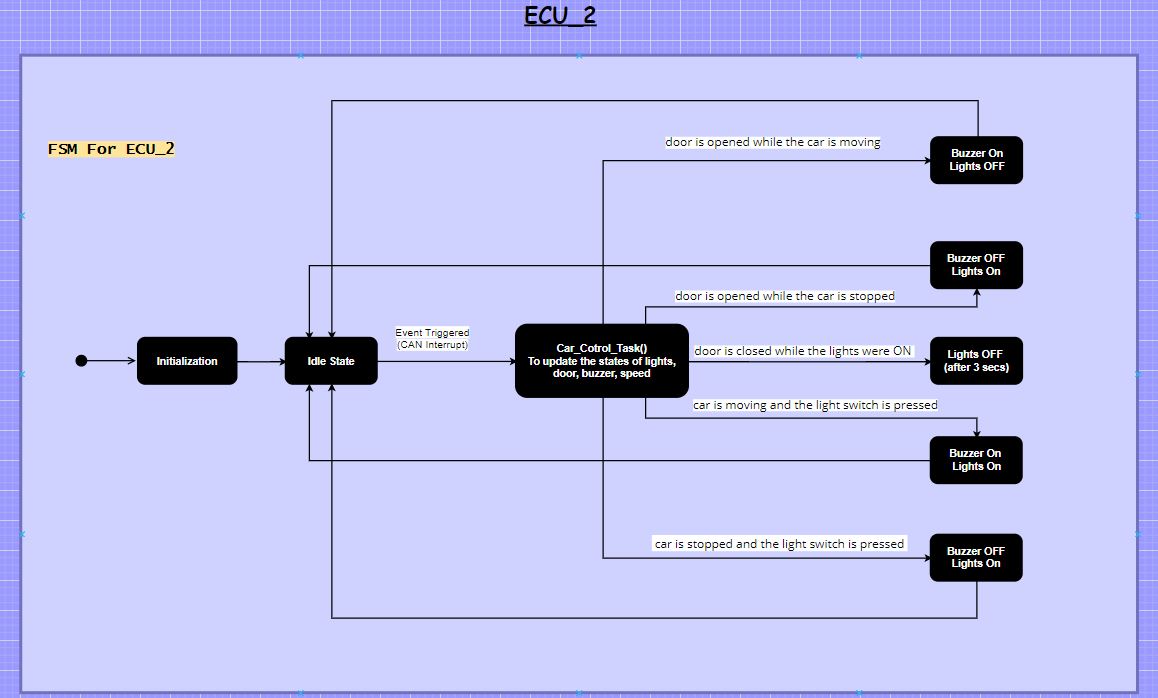
# ECU2:

## FSM for each component of ECU2:

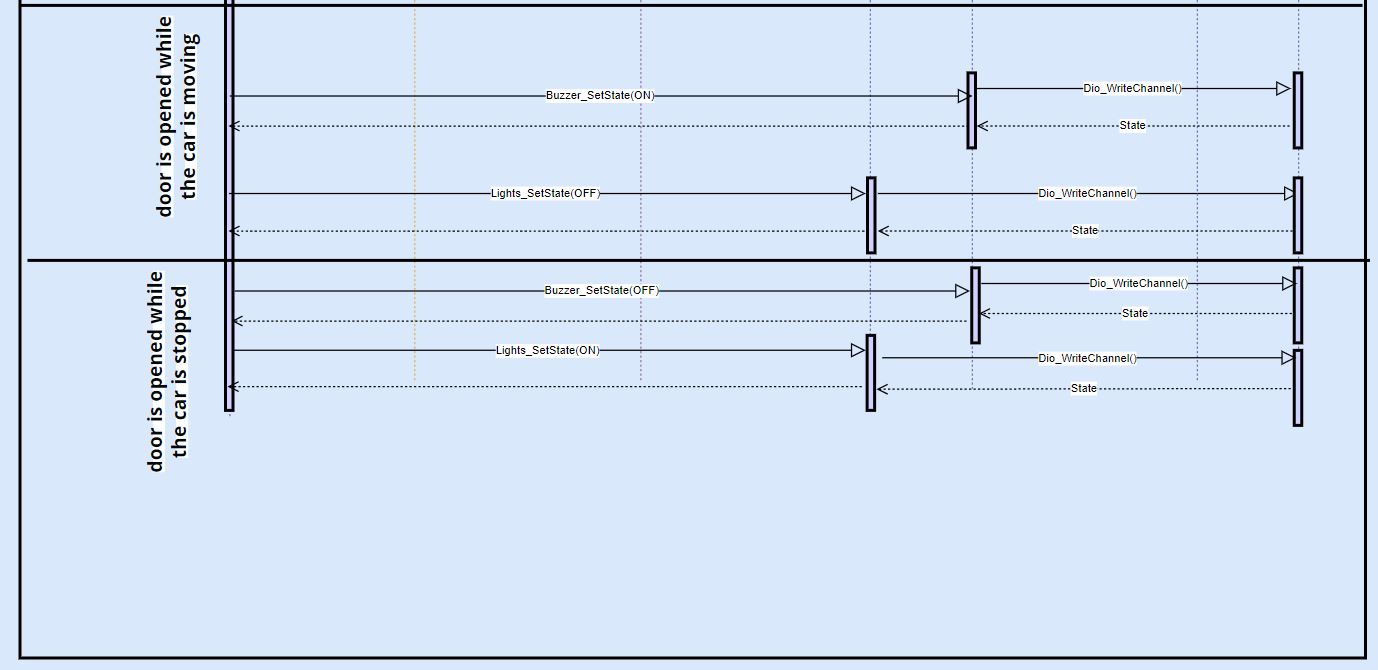
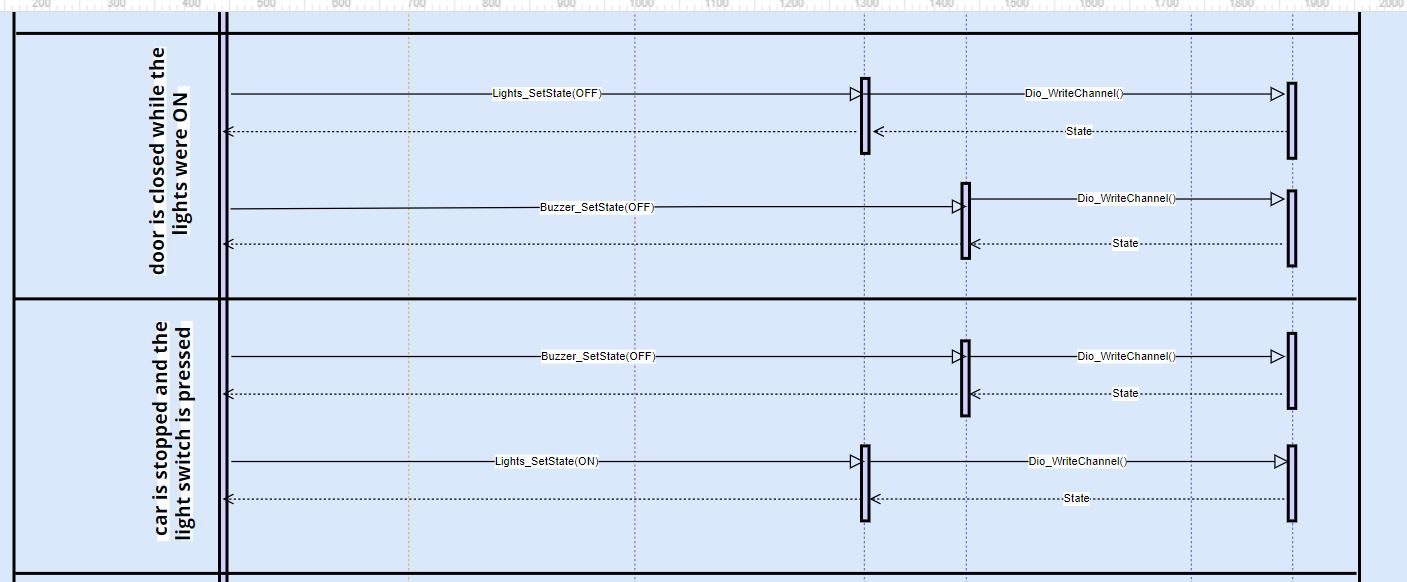
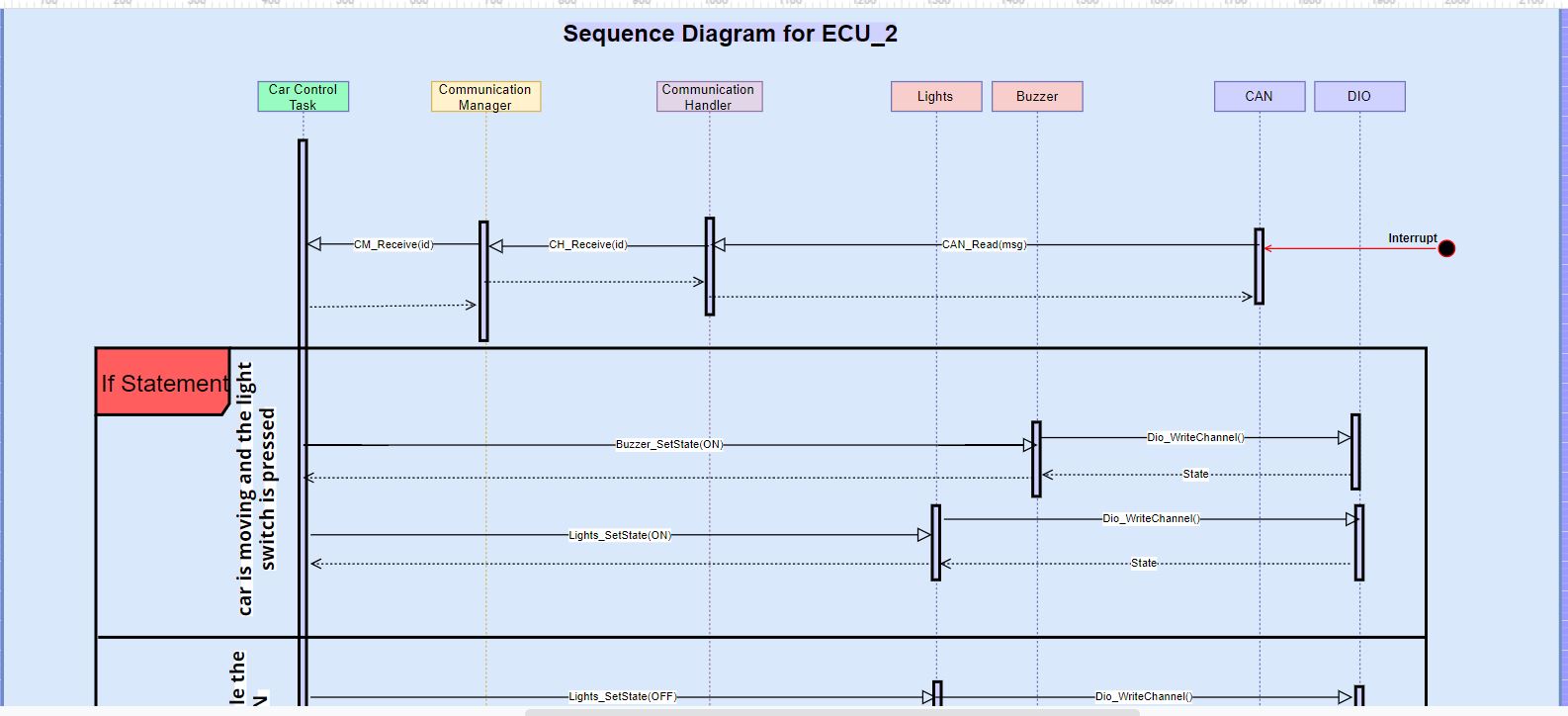


## 

## FSM for ECU2:



## Sequence Diagram:



## CPU Load:

Assuming all tasks execution time = 1ms:

U = (E1)/H = (1 ∗ 1)/5) ∗ 100 = 20%

## Bus Load:

Assume:

Frame = 32bit

Bitrate = 100kBit/s

tframe = 32bit ∗ 1/100 kBit/s = 320us

frames/sec = 1000/5 + 1000/10 + 1000/20 = 350

tbus = 350 ∗ 320us = 112000us = 0.112s

Bus Load = 0.112 ∗ 100 = 11.2%